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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAO, LUN YI	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/805,190	KAWABE ET AL.	
	Examiner	Art Unit	
	Lao Y Lun	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16 and 20-24* is/are rejected.

7)☒ Claim(s) *15 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/2005 &9/13/2005*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-14, 16 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usui et al in view of Sakashita(6,501,451).

As to claims 1-4, 6-14, 16 and 22-23, Usui et al teach a display device comprising a display module(LCD display) and a correction circuit(51, 52)(see figure 8) for receiving a gradation signal (gray scale signal; e.g. 5 bits), generating a correction signal for canceling of a luminance deficit caused by a response delay in the display module based on an (N-1th)(previous frame) and an N-th frame(current frame) input gradation signal; correcting N-th frame input gradation signal using correction signal(output from ROMs(77, 87)) and outputting the corrected N-th frame input gradation signal to an LCD display(see figures 3, 8-9; abstract; column 5, lines 17-68; column 6, lines 1-13; column 8, lines 65-68 and column 9, lines 1-67). Usui et al teach target luminance of the corrected N-th frame(previous frame) input gradation signal overshoots or undershoots luminance of the N-th frame input gradation signal within

one frame interval(see figures 3, 8, 21; abstract; column 5, lines 31-68 and column 6, lines 1-13).

Usui et al fail to disclose a correction circuit for adding/subtracting a luminance signal to the gradation signal of N frame.

Sakashita teaches an LCD display comprising a correction circuit(206 or 406) for adding/subtracting a luminance signal(correction data) of the gradation signal of N frame(see figures 2, 4-6B; column 7, lines 17-29). It would have been obvious to have modified Usui et al with the teaching of Sakashita, so as to reduce the cost of a memory by deceasing the capacity of memory to store the correction data of current frame(see column 8, lines 64-67).

As to claims 3-4, Usui et al teach a correction circuit(5) for decreasing a gradation level of a current image signal if the current image signal is less than the previous image signal(see figures 5-6, 8; abstract; column 5, lines 31-68 and column 6, lines 1-13).

As to claim 6, Sakashita teaches a fram storge module(203) for generating preceding frame gradation signals(see figure 2 and column 7, lines 17-22).

As to claim 13, Usui et al teach a timing control circuit(11); a scan driver circuit(21, 22) and a data driver circuit(23, 24)(see figure 8 and column 8, lines 33-44).

As to claims 14, Usui et al teach correction circuit(51, 52) generated the correction signal based on the correction levels predefined in the correction data table(77, 87)(see figures 8-9 and column 10, lines 24-47).

As to claims 7-8 and 22, it would have been obvious to have a compensation rate for luminance deficits in the correction signal is within -30%-10% for intermediate gradation in three-frame intervals since Usui et al teaches a display device for improve a display quality based on the difference of the luminance levels of present frame and the preceding frame(see figures 4-5; abstract; column 1, lines 48-51; column 5, lines 33-68 and column 6, lines 1-4); and the range of the compensation rate is an obvious design choice since it would depend one the quality of a display should be provide to a user since the compensation rate could be changed(see column 5, lines 43-65).

As to claims 9 and 23, Usui et al teach the correction circuit comprising for edge enhancement(see figure 5 and column 5, lines 35-42).

As to claim 10, Usui et al teach the correction signal generating module generates the correction signal based on a frame frequency or the liquid crystal panel(see figures 7-8 and column 8, lines 5-64).

As to claims 14 and 16, Usui et al teach a correction data table(77,87, 324)(see figures 8-9, 21; column 5, lines 52-68; column6, lines 1-4; column 17, lines 50-68 and column 18, lines 1-21).

3. Claims 1-4, 6-14, 16 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usui et al in view of Uehara et al(6,329,980).

See the discussion of Usui et al above.

As to claims 1-4, 6-14, 16 and 20-23, Usui et al teach an LCD display having storages(73, 74, 83, 84 or 321) for storing preceding and current frame input images

and a subtracter(322)(see figure 21 and column 17, lines 55-66). Usui fails to disclose an adding for adding correction signal to the current frame input gradation signal.

Uehara et al teach an add/subtracter adding and subtracting correction signal and the current frame input gradation signal(see figures 4-12 and column 9, lines 13-61). It would have been obvious to have modified Usui et al with the teaching of Uehara et al, so the current frame correction signals could be calculated instead stored in a memory and reduce the cost of a memory.

As to claim 7, Usui as modified teach the correction circuit(10) for generating a correction signal by linearizing the relationship between the correction signal and a gradation(see Uehara's figure 8(a)-8(g) and column 10, lines 9-49).

As to claims 7-8 and 22, it would have been obvious to have a compensation rate for luminance deficits in the correction signal is within -30%-10% for intermediate gradation in three-frame intervals since Usui et al teaches a display device for improve a display quality based on the difference of the luminance levels of present frame and the preceding frame(see figures 4-5; abstract; column 1, lines 48-51; column 5, lines 33-68 and column 6, lines 1-4).

As to claims 9 and 23, Usui et al teach the correction circuit comprising for edge enhancement(see figure 5 and column 5, lines 35-42).

As to claims 14 and 16, Usui et al teach a correction data table(77,87, 324)(see figures 8-9, 21; column 5, lines 52-68; column6, lines 1-4; column 17, lines 50-68 and column 18, lines 1-21).

As to claim 20-21, Uehara et al teach a correction circuit having a selection circuit(16)(see figure 10; column 11, lines 52-68 and column 12, lines 1-9).

4. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Usui et al(5,465,102) in view of Sakashita or Uehara et al and Shimomura et al(5,406,305).

Usui et al as modified fail to disclose a back-light.

Shimomura et al teach a display device comprising a back light(7)(see figure 1 and column 4, lines 4-26). It would have been obvious to have modified Usui et al as modified with the teaching of Shimomura et al, so the display information could be viewed at night.

Allowable Subject Matter

5. Claims 15 and 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Applicant's arguments with respect to claims 1-4, 6-14, 16 and 20-24 have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue that the combination of Usui fails to disclose (1) add a luminance that enables cancellation of luminance deficit caused by response delay in the display module of gradation level if an N-th frame gradation signal is greater than a gradation level of an (N-1)th frame gradation signal and 2) subtract a luminance that enables cancellation of luminance deficit caused by response delay in the display module of gradation level if an N-th frame gradation signal is greater than a gradation level of an (N-1)th frame gradation signal, the examiner disagrees with that since Usui teaches add a luminance(overshooting)that enables cancellation of luminance deficit caused by response delay in the display module of gradation level if an N-th frame gradation signal is greater than a gradation level of an (N-1)th frame gradation signal(N-th frame signal comparing the N-1th frame signal in Fig. 8) and 2) subtract a luminance(undershooting) that enables cancellation of luminance deficit caused by response delay in the display module of gradation level if an N-th frame gradation signal is greater than a gradation level of an (N-1)th frame gradation signal(see figures 3-5, 8; column 5, lines 36-68; column 6, lines 1-16 and column 9, lines 8-30).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 28, 2005

Lun-yi Lao
Primary Examiner